REMARKS/ARGUMENTS

Applicants wish to thank Examiner for the reading of their Application and to briefly summarize their invention.

The present claimed invention is a double barrier resonant tunneling diode, that is, it is a thin planar layer of semiconductor material (creating a resonant quantum well) formed on a SOI substrate by a process of photolithographic patterning and etching, with a dielectric layer formed by chemical vapor deposition (CVD), atomic layer deposition (ALD) or sputtering, on each of its planar sides (creating the double barrier). Each of the dielectric layers serves as a potential barrier to the passage of conduction electrons through the device, while the semiconductor layer between them serves as a resonant quantum well that creates a discrete set of energy levels that an entering electron must have if it is to have a high probability of passing through. Thus, by varying the height of the dielectric potential barrier layer into which electrons are being injected, an electron having both sufficient energy to overcome the barrier and the right energy to match an energy level within the well, will most likely be able to traverse the device.

The present claimed invention is novel over prior art tunneling diodes in that its double dielectric tunneling barrier layers are formed of particular dielectric materials that have a low band offset relative to the conduction band edge of the semiconductor material forming the quantum well. These use of these materials have been shown by the Applicants to significantly improve the performance of the device. Thus, if the quantum well is formed, for example, of silicon or germanium, the dielectric material can be Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates, as in claim 4. Prior art resonant tunneling diodes have used other materials as barrier layers, but it is

found herein that the combination of these low band offset materials and the silicon or germanium well materials produces a device of particularly good performance as noted in the Application.

Another aspect of the invention, which is described and claimed in claim 10, is the fact that the diode can be advantageously formed using the SOI (Silicon On Insulator) substrates that have become somewhat of an industry standard for use in fabricating integrated circuits. While the use of an SOI as a substrate greatly improves the efficiency and broad applicability of the fabrication methodology, those benefits add to the already substantial advantages resulting from the low band offset barrier layers that are formed on the sides of the quantum well.

Claim Objections

Examiner objects to the wording in claim 1 because of the following informalities: the phrases "a quantum well layer" and "a tunneling barrier layer" should be replaced by their plurals, "quantum well layers" and "tunneling barrier layers." The device claimed in amended claim 1, however, comprises only a single quantum well layer, so replacing it with "layers" would incorrectly describe the invention. An amended phrase, "tunneling barrier layers formed on each side..." could be misinterpreted as claiming more than one such layer formed against each side of the single quantum well layer. Applicants would very respectfully argue that the original wording of claim 1 clearly describes their invention.

Claim Rejections- 35 USC §102

Applicants respectfully request reconsideration of the rejection of claims 1 (as amended), 3 and 10 as being anticipated by Krivokapic (US Patent No. 6,291,832) for the following reasons.

Krivokapic teaches the formation of a resonant tunneling diode latch, which is two resonant tunneling diodes in series. Moreover, Krivokapic teaches the formation of the latch within a SOI substrate, which is the same substrate material claimed in dependent claim 10 of the present claimed invention. According to Krivokapic's Fig. 5 and his description in lines 3-6 of column 4, the "thin portions of undoped silicon 208 lay between the n+ doped region 204 and the p+ doped regions 206 and serve as tunneling barriers". Krivokapic uses the same language in his claim 1, namely in lines 11 and 12, "...the tunneling barrier being an undoped portion of the silicon substrate."

In the language of the present claimed invention, the claimed barrier layers are the low band offset dielectric layers formed on either side of the quantum well, providing a potential barrier to injected electrons. Krivokapic does not have such low band offset dielectric barriers in his invention. In the present claimed invention, biasing the barrier layers controls the flow of conduction electrons to the quantum well. Krivokapic discloses no such dielectric barrier layers to go along with his quantum well. Therefore his invention is fundamentally different from the present claimed invention.

Applicants would, therefore, suggest that the diode of Krivokapic is not a double barrier resonant diode as claimed in the present application because it does not have dielectric barrier layers disposed against the sides of the quantum well layer, as can be seen in Fig. 5. In addition to the lack of the low band offset dielectric barrier layers, Krivokapic's invention differs in yet another significant way from the present claimed invention. In Krivokapic's device, as illustrated in his Fig. 5, there are two diodes formed in a back-to-back configuration. One diode is p^+ Si to undoped Si to n^+ Si (shown as regions 206, 208 and 204 in Fig. 5), the second diode is n^+ Si to undoped Si to p^+ Si, (shown as regions 204, 208 and 206 in Fig. 5). This construction is discussed in column 3, lines 63-68 and column 4, lines 1-6 of Krivokapic. In the present claimed invention, there is only one diode and any similarities between Fig. 7 of the present Application and Fig. 5 of Krivokapic are purely superficial. The operational principles of Krivokapic's back-to-back diodes and the present claimed diode with low band offset barrier layers are completely different.

Applicants would, therefore, respectfully argue that Krivokapic's invention is not the present claimed invention, but is rather a formation of two prior art single barrier resonant diodes formed in series. Krivokapic's invention does not teach or disclose the low band offset dielectric barrier layers that are one of the novel aspects of the present claimed invention.

Further yet, the tunneling barrier described and claimed by Krivokapic is not a layer formed by a photolithographic patterning and etching process in the sense of amended claim 1 of the present claimed invention, rather it is an undoped region between two doped regions within a SOI substrate (region 208 in Krivokapic's Fig. 5). Thus its

planarity would be affected by the diffusive nature of doping. Therefore, when claim 1 of the present claimed invention claims the formation of a photolithographically patterned and etched layer having parallel, planar vertical sides (line 8 of present claim 1), such a layer is not the layer of the invention described or claimed by Krivokapic. Similarly, in the present claimed invention the dielectric barrier layers formed of low band offset material are formed by a deposition process of CVD, atomic layer deposition or sputtering. Such barrier layers are neither formed nor do they exist in the invention of Krivokapic, where the only structures abutting his vertical layer 208 in his Fig. 5 are the doped regions 206 and 204 within the body of the SOI substrate.

For the reasons described above, Applicants respectfully argue that their claims 1 and 3 are not anticipated by the invention of Krivokapic. Similarly, Applicants respectfully argue that their claim 10, goes well beyond any description or claims of Krivokapic. While Krivokapic does form his latch configuration within a SOI substrate, his configuration is formed by a doping process that defines his barrier layer. In the present claimed invention, the SOI substrate is used to create the quantum well layer through a photolithographic etching process and the dielectric layers are not formed from the SOI substrate material, but are formed on the well layer by various deposition processes using material not taken from the SOI substrate. For example, this fabrication method is compatible with the technology of CMOS FinFet structures, which is highly desirable. Thus, the SOI substrate is used differently by Krivokapic and the present Applicants. Moreover, although an SOI substrate is used by both Krivokapic and the present inventors, the final configuration formed thereon is patentably different. Therefore, the present Applicants respectfully argue that they can claim (in claim 10) the

use of the SOI substrate with which to form their invention and not be anticipated by Krivokapic.

Claim Rejections- 35 USC §103

Applicants respectfully request reconsideration of the rejection of claims 2 and 4-9 as being unpatentable over Krivokapic for the following reasons. Examiner argues that Krivokapic teaches substantially the entire claimed structure of the present Applications. Applicants would respectfully point to their previous argument in which they have shown that the invention of Krivokapic is distinct from the present claimed invention. Applicants would argue, in particular, that one skilled in the art would find no place in Krivokapic's invention to apply low band offset dielectric layers. Since the quantum well layer of Krivokapic is formed internally as a region that is undoped, dielectric layers could not be formed about it, nor would the formation of such low band offset layers be suggested by Krivokapic.

Claim 2 of the present claimed invention claims a quantum well layer of Si, Ge or SiGe. As discussed above, the layer claimed in the present invention is not the same layer claimed by Krivokapic, since his layer is an undoped region within the body of the SOI substrate, while the present claimed layer is an etched layer of Si (or Ge or SiGe).formed on (rather than within) a SOI substrate.

Applicants have amended claim 1 to clarify the description of their invention by reciting a photolithographically etched semiconductor layer and dielectric layers formed by CVD, ALD or sputtering. These limitations are already present in the Specification and do not constitute new matter.

Applicants agree with the Examiner that the prior art made of record and not relied upon does not suggest the present claimed invention.

If the Examiner has any questions regarding the above application, please call the undersigned attorney at 845-452-5863

Respectfully submitted,

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